NAND Flash - The New Era of 4 bit per cell and Beyond

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Based on the latest NAND products that Semiconductor Insights has analyzed thus far and compiling the information published in International Solid State Circuits Conference (ISSCC) 2009 papers in early February, we were able to identify the challenges and innovations of NAND Flash manufacturers made to weather the storm of the difficult economic times currently affecting them.

The most notable of features to the latest designs announced at ISSCC 2009 is 3 bit-per-cell and 4 bit-per-cell designs from Toshiba, SanDisk and Hynix which have advanced NAND Flash cell efficiency dramatically. NAND Flash industry has entered into an era of more than 250Mbit per mm2 of NAND die efficiency with the combination of advanced process technologies in 40 nanometer(nm) and 30nm class and innovative programming techniques supporting three and four bits per NAND Flash memory cell.

Compared to the efficiency in the range of 100 ~ 150Mbit per mm2 with 50nm and 40nm process and MLC (two bit per cell) technology released less than a year ago, this achievement is phenomenal given the continued price decline and the widespread struggle of the whole memory industry.

The overall architectures also show different choices that NAND manufacturers made. Toshiba and SanDisk designs are utilizing their ABL (All Bit Line) architecture that they introduced a year ago in all of their new designs. Samsung's 42nm design is based on its traditional architecture - using even and odd bit-lines separately. Hynix's 48nm 3 bit-per-cell 32Gbit NAND design also uses conventional bit-line architecture with two planes. Intel and Micron have adopted an architecture which has page buffers placed in the center of the die effectively reducing bit-line length and load in half-enhancing performance.

Since the introduction of the 40nm class process node, the reliability of a NAND cell under severe programming conditions has been one of the top priorities for NAND Flash developers. Different vendors adopted different ways to achieve the reliability while reducing the overhead of the added measures.

Toshiba and SanDisk have adopted two dummy word-lines (one on each end of a NAND string, next to select gates) to alleviate the electrical stress and achieve the level of reliability for the cells prone to degradations and failures due to Gate Induced Drain Leakage(GIDL). To minimize the overhead of the added word-lines to the die size, the size of NAND string has been doubled to 64 from traditional 32. The resulting size of NAND string with two dummy word-lines has become 66 (64 + 2). As a result of this architectural choice to achieve reliability of NAND cells, the bit-lines have become twice as long as they would have been had the NAND string size not been modified. Innovative driving of the control gate to alleviate this effect was adopted in NAND Flash by this new architecture. Toshiba and SanDisk maintained this NAND string structure developed in their 43nm product line (analyzed and confirmed by Semiconductor Insights' analysis) with their 32nm 3 bit-per-cell 32Gbit NAND design and 43nm 4 bit-per-cell 64Gbit NAND design as well.

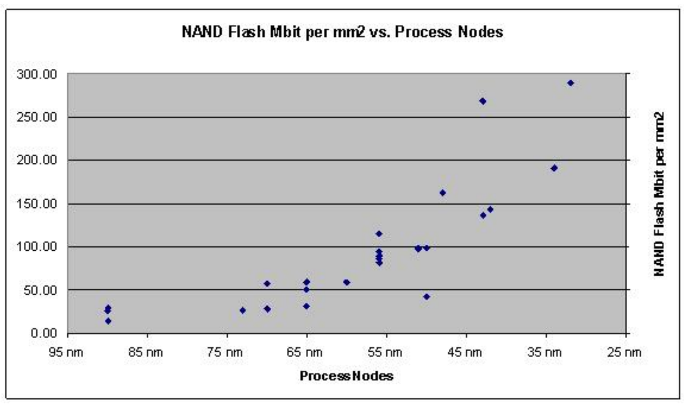

Figure 1. Trend of NAND Flash cell efficiency

3 bit-per-cell and 4 bit-per-cell designs come with challenges. The first and most obvious issue is how to place the states with 8 different states for 3 bit-per-cell design and 16 different cell threshold voltage states in a cell in the case of 4 bit-per-cell design. From a circuit design standpoint, this means higher levels for internal voltage pumps to generate. Voltage pumps take a large portion of any NAND Flash die - even for MLC. With the requirement of generating higher voltage levels than before, voltage pumps for 3 bit-per-cell and 4 bit-per-cell NAND designs require higher efficiency and reliability,

which are key factors for successful NAND product development.

Programming these 8 or 16 different states into individual a NAND Flash cell is critical in achieving high performance. ISSPP based programming methods have been widely used in MLC design in the past. New and innovative programming techniques presented in the latest NAND Flash designs have to be optimized for stability of operation and achieving reasonably performance required for the target applications. Increased NAND string size also affects how the word-line voltages are generated and applied to them depending on their relative position in a NAND string. DAC type voltage regulator control for inhibit voltage generator in the Intel and Micron's 34nm 32Gbit NAND Flash is an example. Improvements over 30% have been reported by Hynix with new programming algorithm called Start Bias Control and Smart Blind Program.

The programming performance of 3 bit-per-cell and 4 bit-per-cell NAND Flash designs varies from design to design but is generally at, or around, 5.5MB/s. Toshiba and SanDisk's 43nm 64Gb 4 bit-per-cell NAND shows 5.6MB/s. Hynix's 48nm 3 bit-per-cell 32Gb NAND Flash has 5.5MB/s. This is in contrast to the performance presented by Toshiba and SanDisk one year ago at ISSCC 2008 with their 56nm 3 bit-per-cell 16Gb NAND design having 8MB/s of performance. In case of Toshiba and SanDisk, despite the 4 bit-per-cell programming challenge and the increased NAND string size, the programming performance of 4 bit-per-cell NAND design shows fairly comparable performance with that of Hynix's 3 bit-per-cell design.

To date, three 3 bit-per-cell NAND Flash designs have been reported in 56nm, 48nm, and 32nm process nodes. 2009 is the first year that the industry finally developed 4 bit-per-cell NAND Flash. This had been anticipated for many years since SanDisk's acquisition of MSystems in July of 2006. Given the challenges of placing 16 different states into smaller cells, the role of the embedded controller IC in NAND products will become even more critical for successful adoption of 4 bit-per-cell based NAND products in broader application areas.

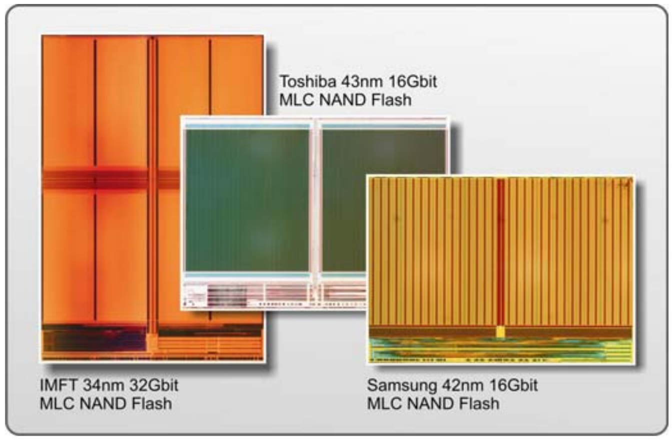

Figure 1 The latest NAND Flash devices from Intel Micron, Toshiba and Samsung (Actual Die Photos)

NAND Flash memory industry has been under tremendous amount challenges from both technological innovation needs to overcoming scaling limitations as well as market challenges due to unfavorable pricing for the last couple of years. The resilience of this NAND industry, and perhaps the memory industry in general, comes from the amount and pacing of innovations that the designers and process/device engineers make every year to overcome seemingly insurmountable obstacles. Looking at the trend of cell efficiency of NAND Flash, one cannot help but notice the amount of improvements that the industry has made in the last 12 months. This is what keeps the industry going despite the cyclical nature of the memory market.